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recent past, the semiconductor industry has experienced technological advances that have permitted dramatic increases in circuit density and complexity, and such advances have made possible the manufacture of both large-scale semiconductor devices and more complex integrated circuits (ICs). One advance that has permitted such increases in complexity is the manufacture of dynamic random access memories (DRAMs). The ability to construct smaller and denser circuits increases the speed at which data can be accessed and/or transmitted, making higher density DRAM circuits a desirable technology for contemporary applications. However, as the circuit density of

DRAM devices has increased, the widths of the wordlines and bitlines that form the storage capacitors and the sizes of the storage nodes that receive the data stored by the storage capacitors have decreased. Conventional efforts to reduce the size of storage nodes and wordlines result in greater distances between successive storage capacitors that, in turn, results in increased electrical coupling between the storage capacitors and the wordlines. Electrically coupling the storage capacitors to the wordlines results in significant stability problems, such as disturb and decay, during the read and write operations of the memory device. 50b96ab0b6

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